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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,492	01/15/2004	Hae-Jeung Lee	P56928	4160
7590	01/26/2006			EXAMINER
Robert E. Bushnell Suite 300 1522 K Street, N.W. Washington, DC 20005-1202			BRINEY III, WALTER F	
			ART UNIT	PAPER NUMBER
			2646	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/757,492	LEE, HAE-JEUNG
	Examiner Walter F. Briney III	Art Unit 2646

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 10 November 2005.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-6 and 8-12 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-6 and 8-12 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 15 January 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1-6 and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi (US Patent 5,220,597).**

**Claim 1** is limited to a *key signal scanning apparatus of a complex telephone operated by using external power and by using a loop voltage when the external power is not supplied*. Horiuchi discloses a dialing apparatus for a power failure extension telephone set of a key telephone system. See Abstract. The dialing circuit includes a control (19) that is powered by a voltage  $V_1$ , generated by a stabilizer (12) from a 24V supply (29) receiving a commercial power supply voltage (i.e. *using external power*). See figure 2 and column 4, line 54, through column 5, line 8. When commercial power supply voltage is lost due to any number of external events, the relay circuits (6), (13a) and (52) alternatively supply subscriber loop DC feed to a power circuit (57), which in turn generates a secondary voltage  $V_2$  for powering the dialing apparatus (i.e. *using loop voltage when the external power is not supplied*). Horiuchi discloses that the combined presence of both commercial and loop voltages requires that safeguards be in place to keep each power network isolated from each other. To this end, figure 5 illustrates an apparatus for scanning a keypad matrix using either the control circuit (19)

or the dialing signal transmit circuit (20). In particular, the keypad matrix (31/32) includes a plurality of rows and columns with a plurality of keys (0-9, \* and #). It is noted that the terms column and row as recited are relative terms, merely distinguishing a correspondence between the elements thereof, but do not indicate a physical orientation such as vertical or horizontal per se. With respect to the claimed subject matter, the control circuit (19) corresponds to the *main microprocessor* as it operates using the commercial power supply (i.e. *external power*) and the dial signal transmit circuit (20) corresponds to the *sub microprocessor* as it operates *when external power is not supplied*. Both microprocessors operate by supplying sequential pulses to the keypad matrix (32) on lines (33) and detecting a closed circuit path signal over lines (34), the sequential pulses corresponding to the *timing signal* and the closed circuit signal corresponding to the *key signal*. See column 6, lines 36-68. As noted above, the two microprocessors are isolated from each other. One element for obtaining isolation is the diode matrix (22), which corresponds to the *first separator circuit* as claimed because it prevents current flow from the output of the main microprocessor to the output of the sub microprocessor. A second element for obtaining isolation is depicted in figure 6 as MOS pass gate (211) and corresponds to a *second separator circuit*.

Please note that the *row output ports and column input ports* of the microprocessors correspond to the column and row ports, respectively, of the control and dial signal transmit circuits disclosed by Horiuchi. Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 2** is limited to *the key signal scanning apparatus of claim 1*, as covered by Horiuchi. Figure 6 includes a second MOS pass gate (212) that corresponds to a *third separator circuit* because it prevents current flow between the inputs of circuits (19) and (20) based on the presence of external power as evidenced by the signal  $V_1$  (i.e. *external power*) being connected to the gates of the pass gate. Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 3** is limited to *the key signal scanning apparatus of claim 2*, as covered by Horiuchi. The pass gate circuit (212) that comprises each individual switch depicted in the control switch circuit (21) of figure 5 (i.e. *connected to each column port of the keypad and to each column port of the sub microprocessor*) is considered a *resistive element* because of its intrinsic effect on current flow and its ability to isolate the processors (19) and (20). Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 4** is limited to *the key signal scanning apparatus of claim 2*, as covered by Horiuchi. As seen from figure 6, the *second separator* (211) has one side connected to the *main microprocessor* (19) and a second side connected to the keypad outputs as well as the first side of the *third separator* (212), which has a second side connected to the *sub microprocessor*. Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 5** is limited to *the key signal scanning apparatus of claim 1*, as covered by Horiuchi. The diode matrix (22) corresponding to the *first separator circuit* clearly couples the output of the control circuit (19) with each anode of each diode, while the cathodes of the diodes couple with the keypad matrix (32). Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 6** is limited to *the key signal scanning apparatus of claim 1*, as covered by Horiuchi. The CMOS circuits are responsive to bipolar inputs, thus corresponding to *bipolar transistor elements* connected as recited. Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 8** is limited to *the key signal scanning apparatus of claim 1*, as covered by Horiuchi. As seen in figure 5, the *first separator circuit* (22) has its input connected to the output of the *main microprocessor* (19) and its output connected to the keypad matrix (32) as well as the output of the *sub microprocessor* (20). Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 9** recites essentially the same limitations as claim 2, as covered by Horiuchi, with the exception that only two separator circuits are claimed. As understood, the first separator of claim 9 corresponds to the second separator of claim 2 and the second separator of claim 9 corresponds to the third separator of claim 2. Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 10** is limited to *the key signal scanning apparatus of claim 9*, as covered by Horiuchi. As shown in the rejection of claim 3, Horiuchi discloses resistive elements (212) connected in circuit as claimed. Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 11** is limited to *the key signal scanning apparatus of claim 9*, as covered by Horiuchi. As shown in the rejection of claim 4, Horiuchi discloses a separator connected as claimed. Therefore, Horiuchi anticipates all limitations of the claim.

**Claim 12** is limited to *the key signal scanning apparatus of claim 9*, as covered by Horiuchi. As shown in the rejection of claim 6, Horiuchi discloses bipolar transistor elements as claimed. Therefore, Horiuchi anticipates all limitations of the claim.

### ***Response to Arguments***

Applicant's arguments filed 10 November 2005 have been fully considered but they are not persuasive.

**With respect to claims 1, 2 and 9**, the applicant alleges on pages 11-14 of the current response that Horiuchi does not disclose a multitude of claim elements, to which the examiner respectfully disagrees. It appears that the alleged differences between the claimed invention and the prior art stem from the claims' usage of the terms "column" and "row" in a manner that contrasts the prior art's usage. However, in rejecting these claims, the examiner noted on page 3, line 24, through page 4, line 3, that the terms "column" and "row" merely establish a two-dimensional orientation between elements (i.e. the key in column 1, row 2, is different than the key in column 2, row 2). Thus, the alleged difference stems from an arbitrary choice of naming. The rejection should be read such that the "columns" of Horiuchi correspond to the "rows" of the claim and such that the "rows" of Horiuchi correspond to the "columns" of the claim. This point notwithstanding, it would have been obvious to simply rearrange parts to arrive at the claimed invention because the reorientation of the matrix 31 so that the columns and rows thereof were respectively aligned with the rows and columns of the

control and dial signal transmit circuit would not result in any new, different or unexpected functions or results.

The applicant alleges that the second and third separator claimed are not disclosed by Horiuchi. The applicant however is not even considering the operation of the CMOS switches 211 and 212 in the same context as applied in rejecting the claim. Specifically, the claims recite the second separator's operation during periods when external power is not supplied. The applicant, however, addresses the operation of switch 211 when power is supplied. Likewise, the claims recite the third separator's operation during period when external power is supplied. The applicant, however, addresses the operation of switch 212 when power is not supplied. In view of the above, the rejections of claims 1, 2 and 9 are maintained.

All other claims not expressly treated supra are maintained for the same reasons.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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SUPERVISORY PATENT EXAMINER

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